

Figure 1

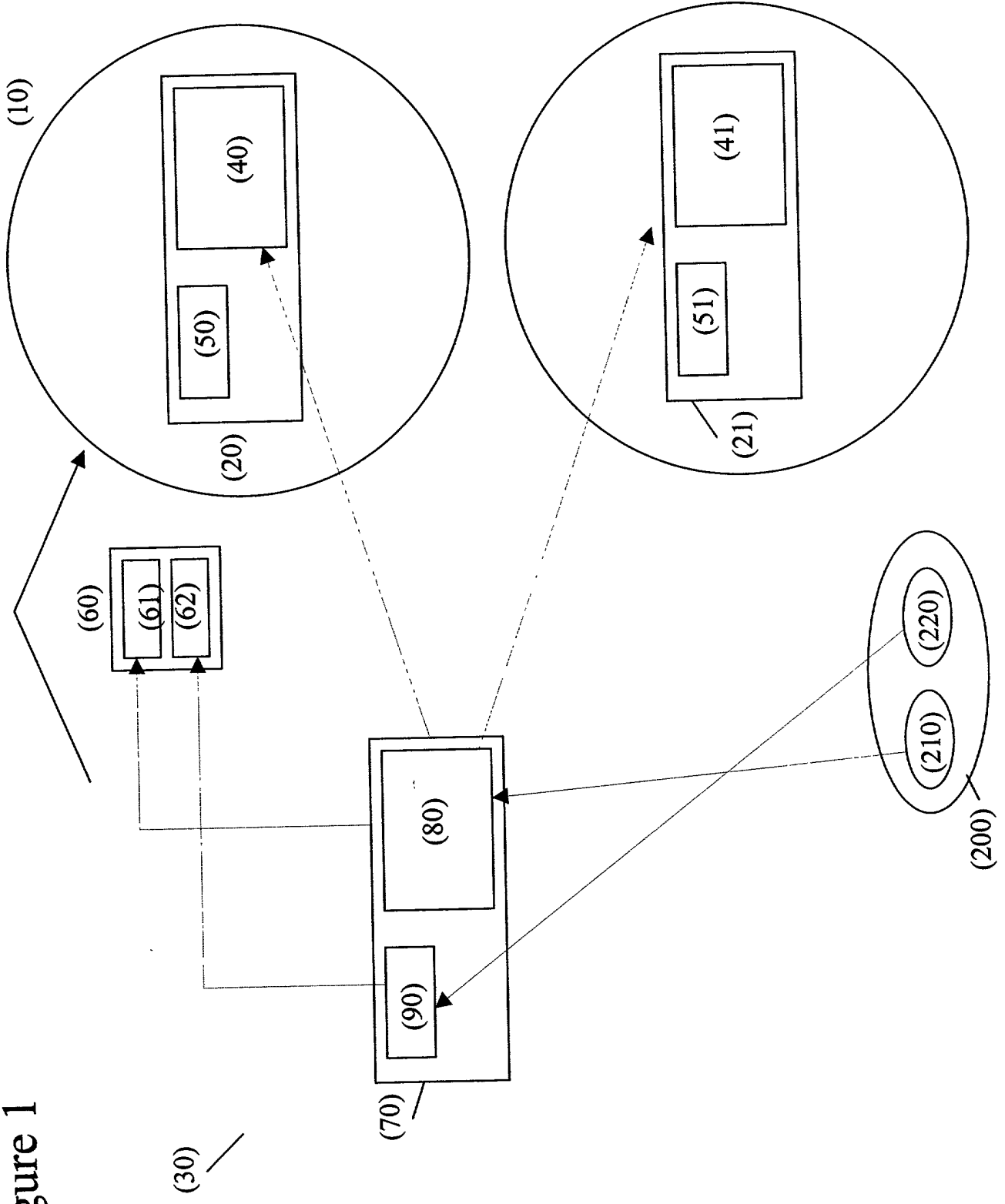
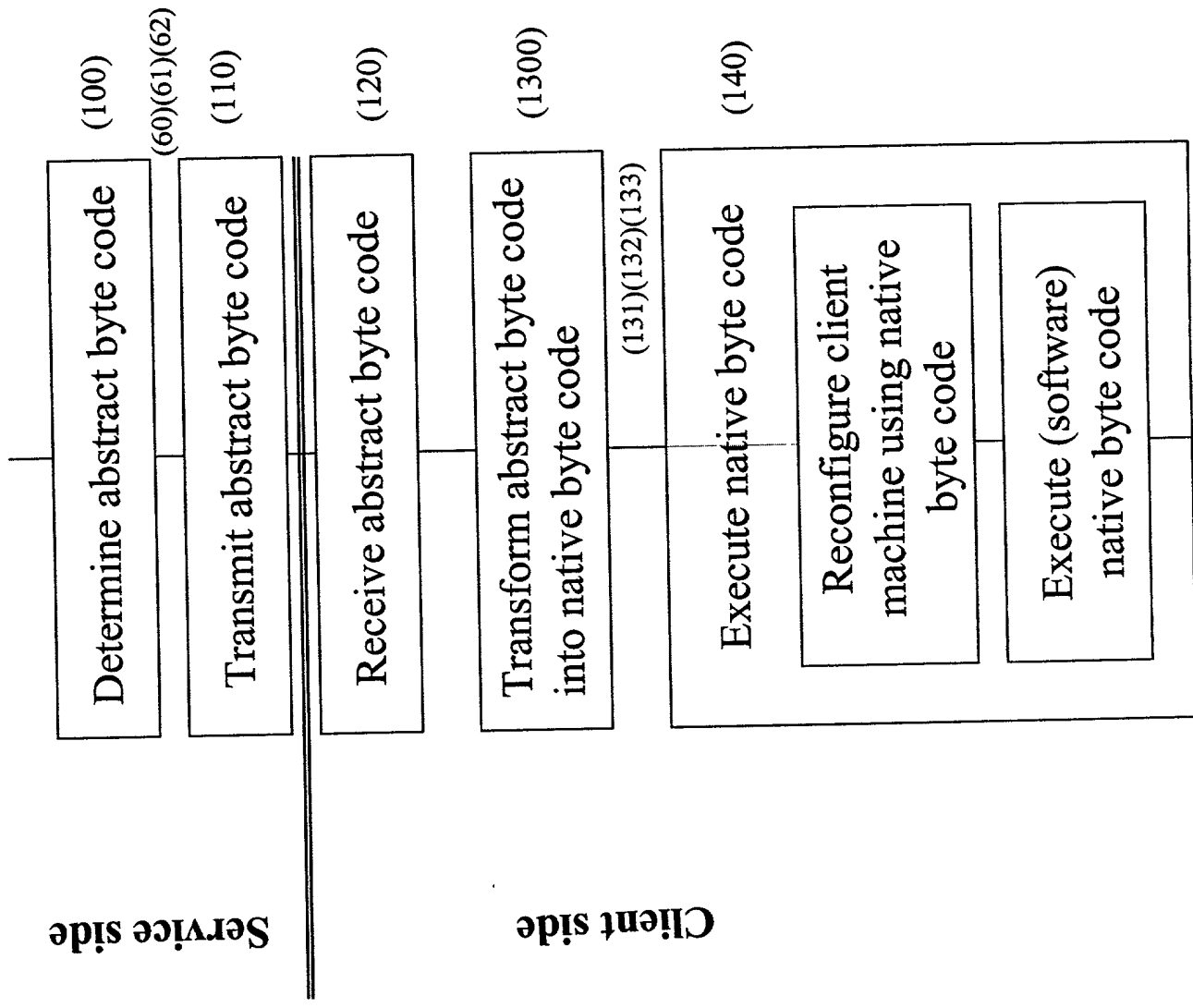


Figure 2



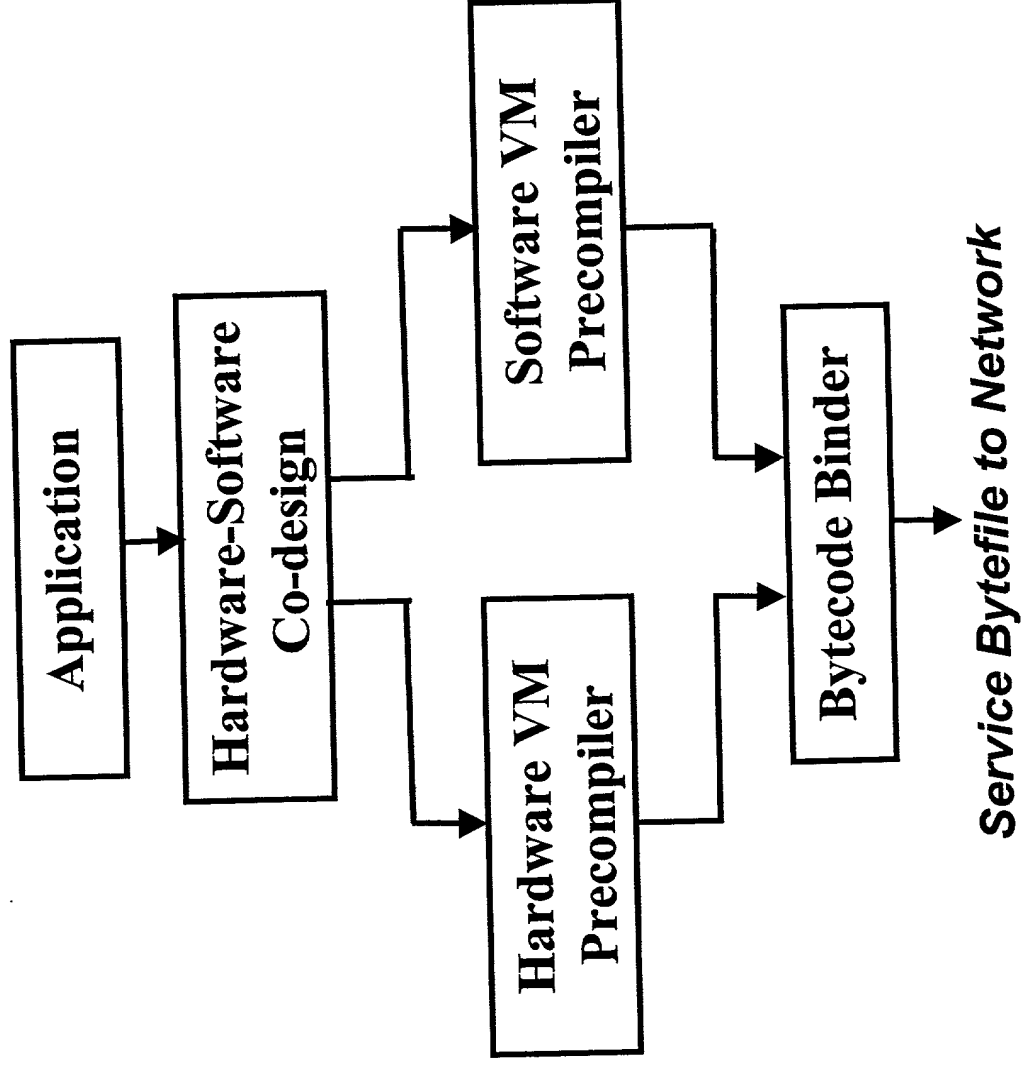


Figure 3

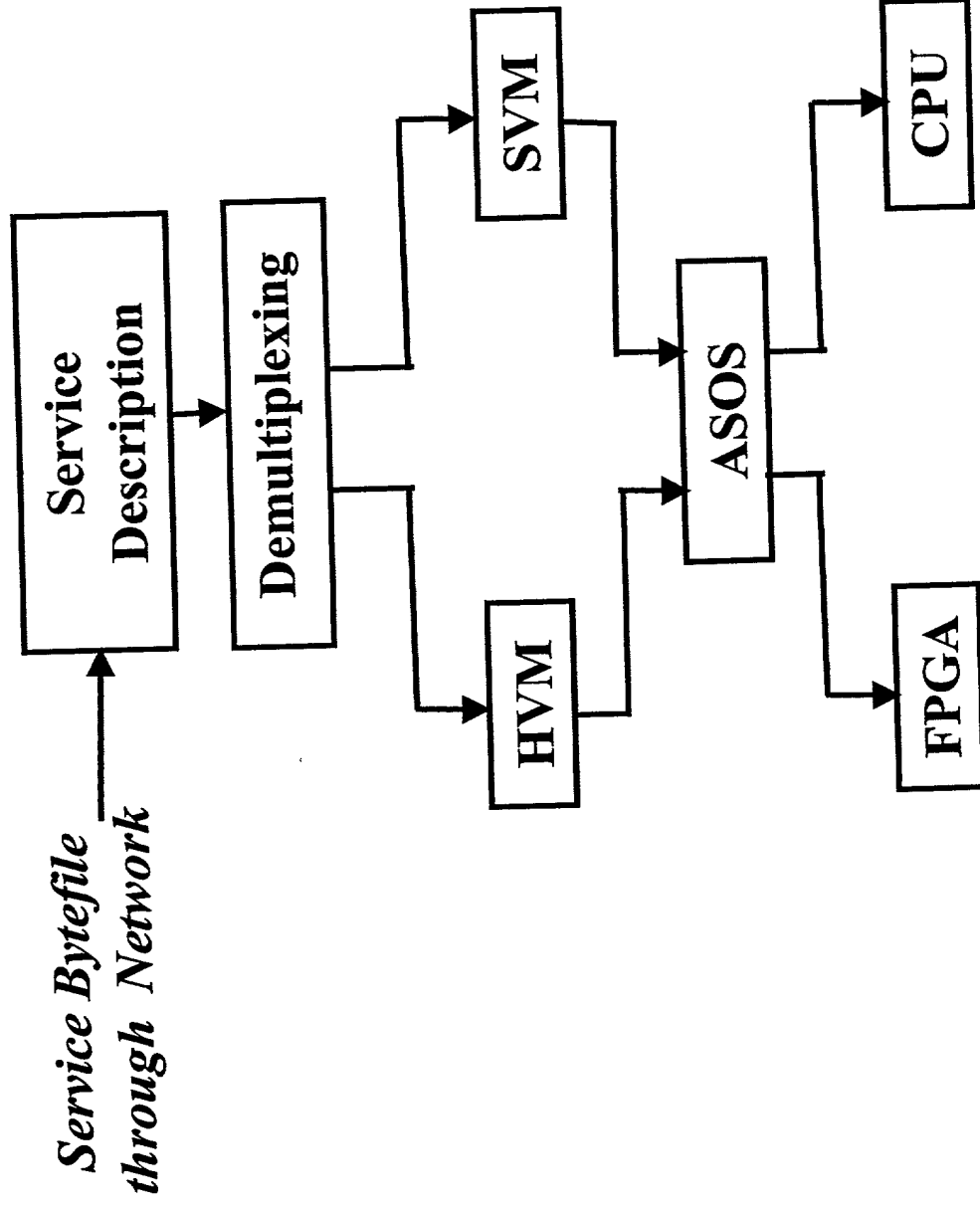


Figure 4

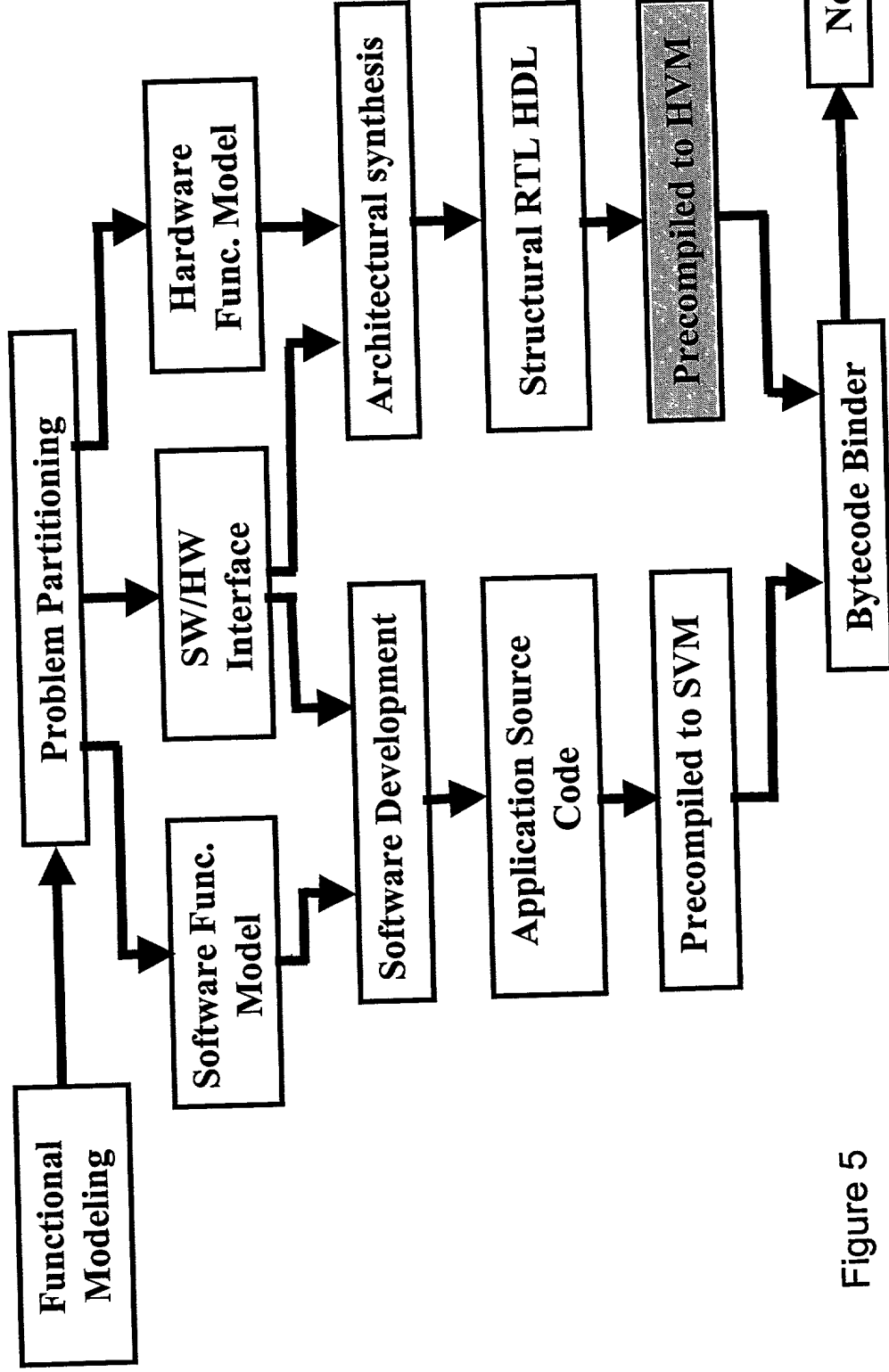


Figure 5

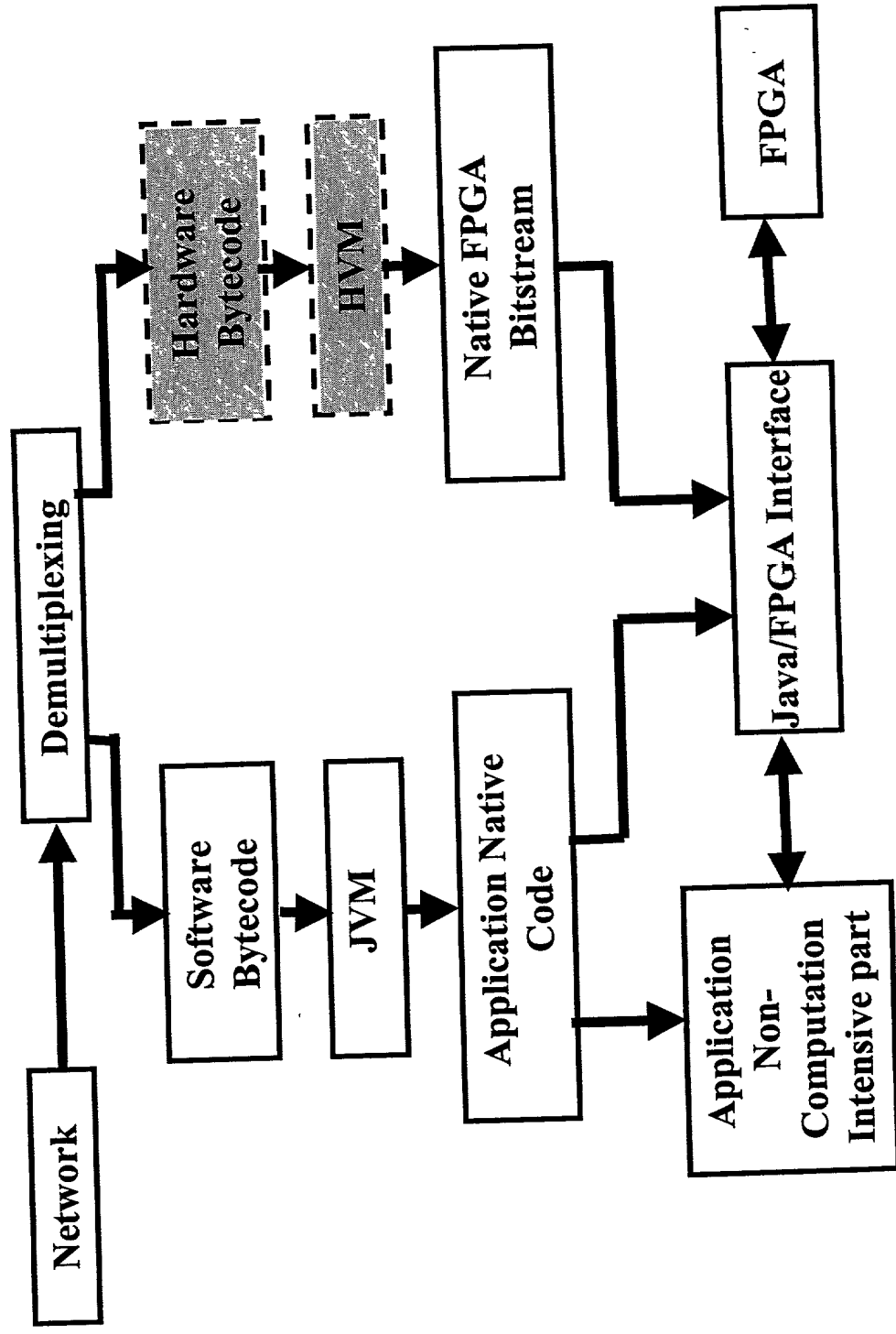


Figure 6

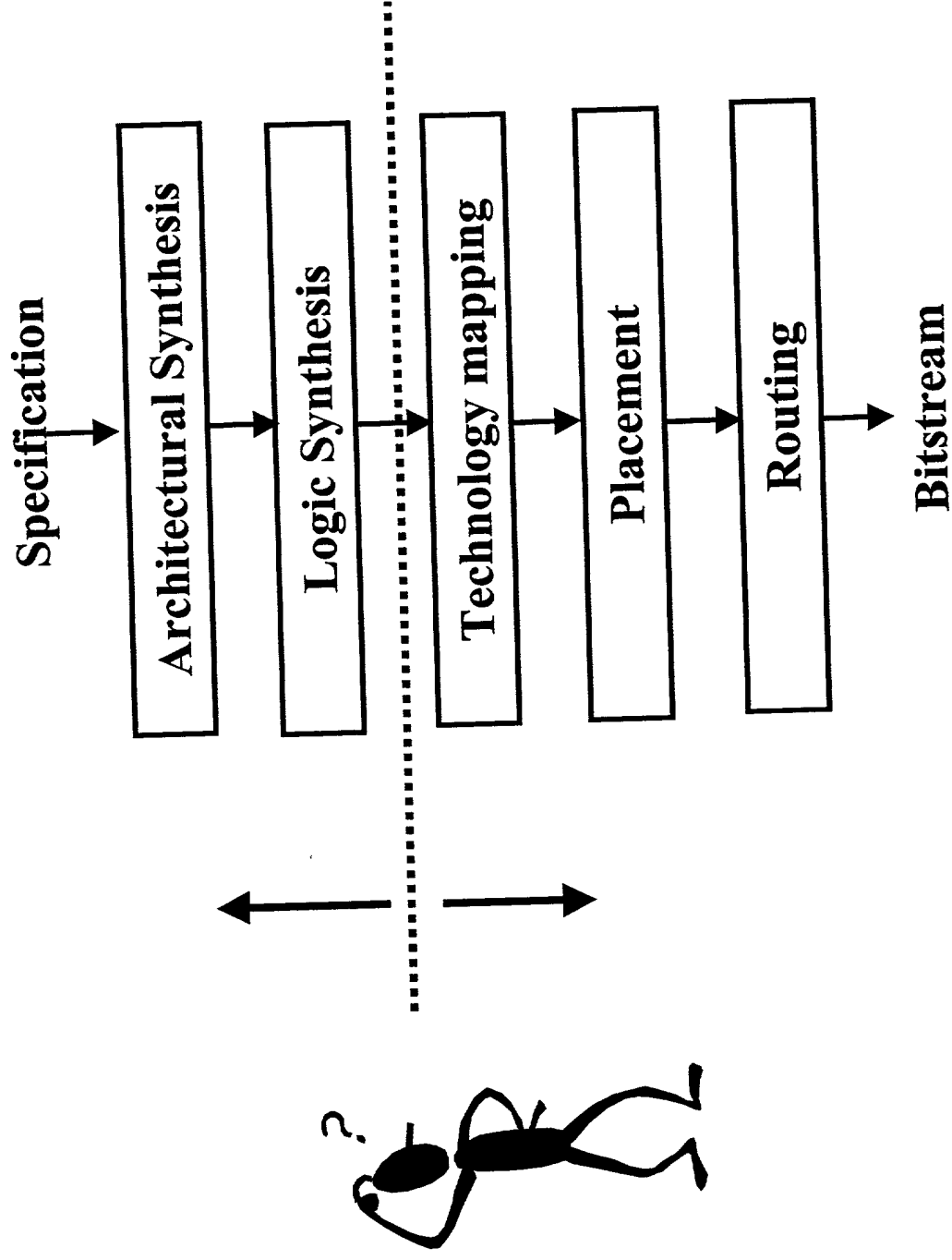


Figure 7

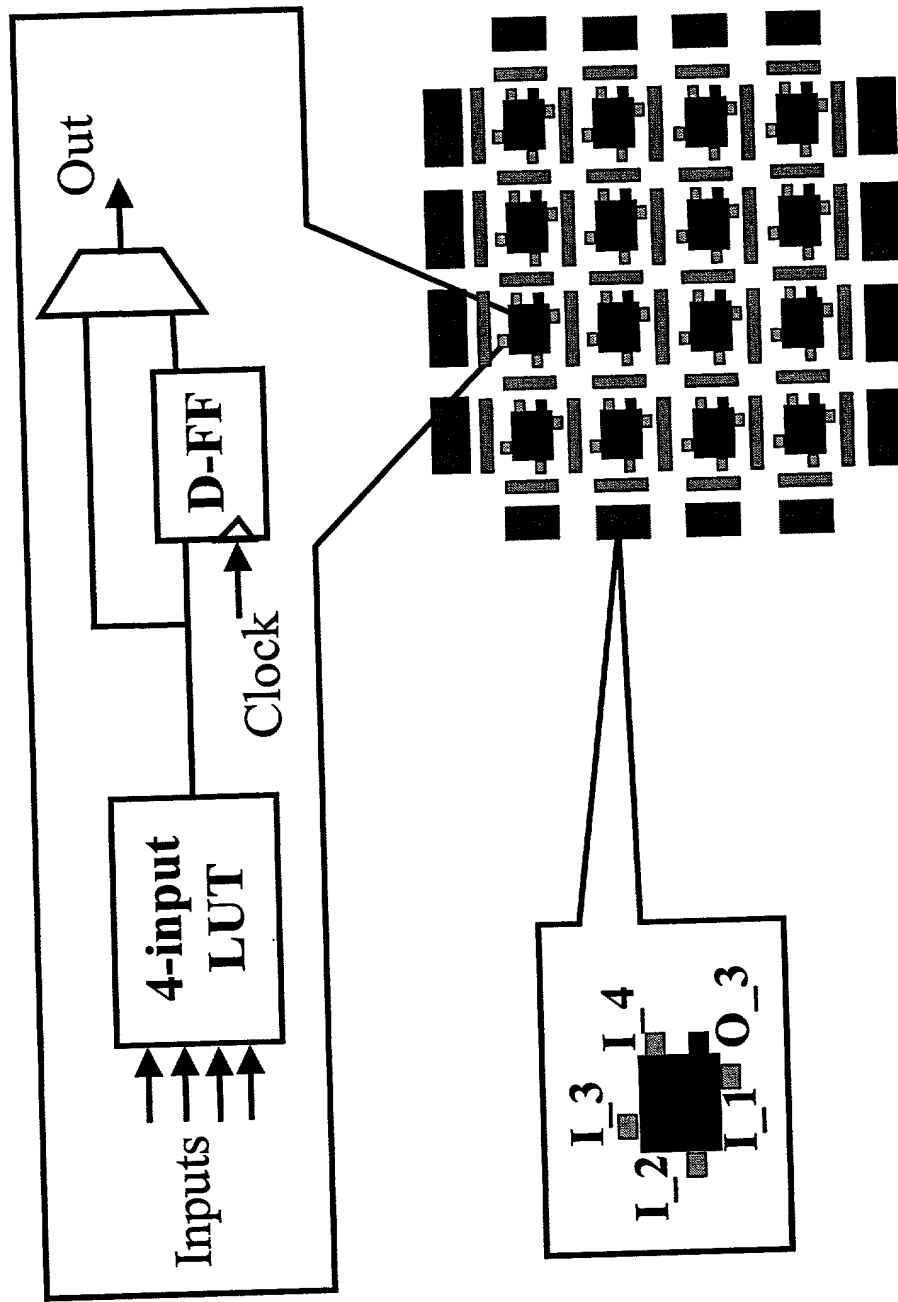


Figure 8



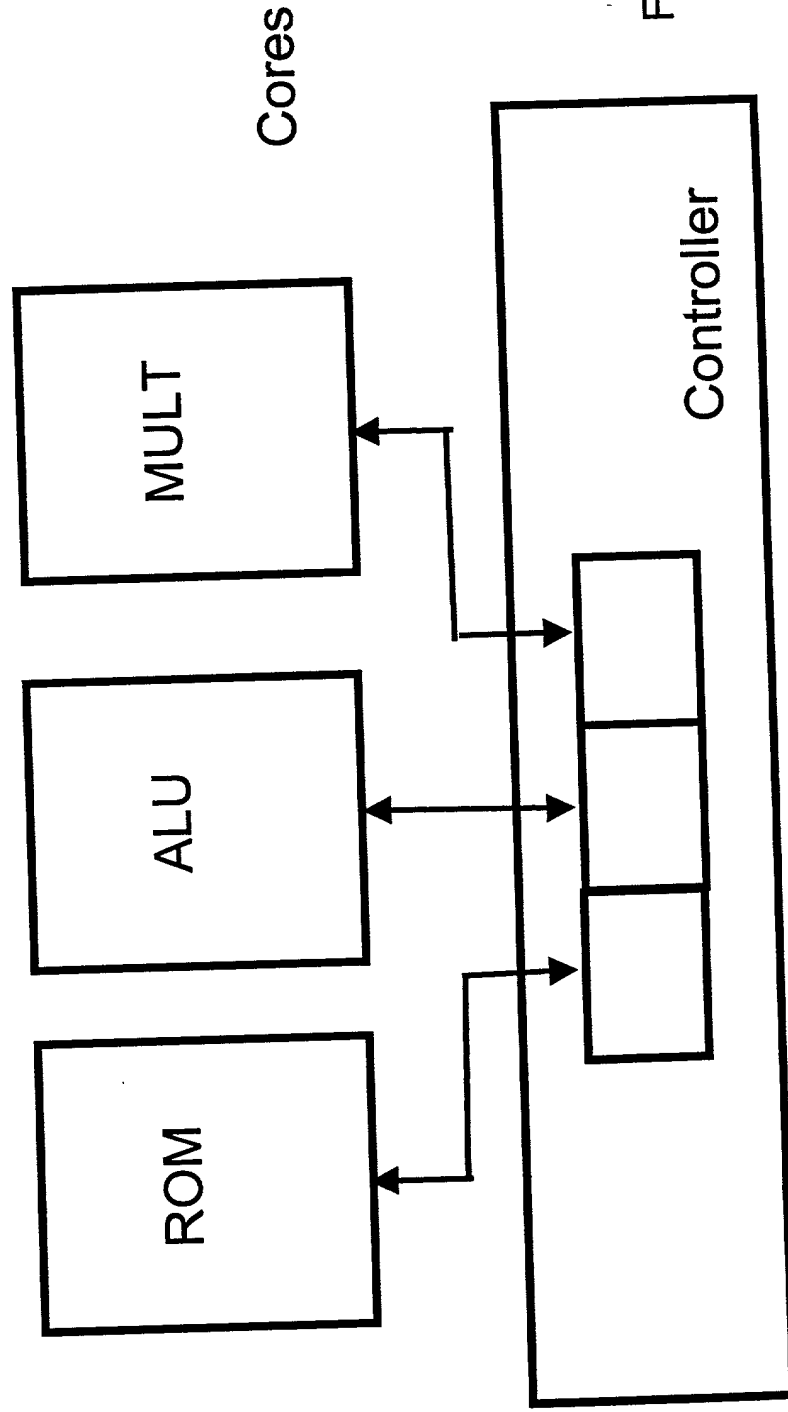


Figure 9

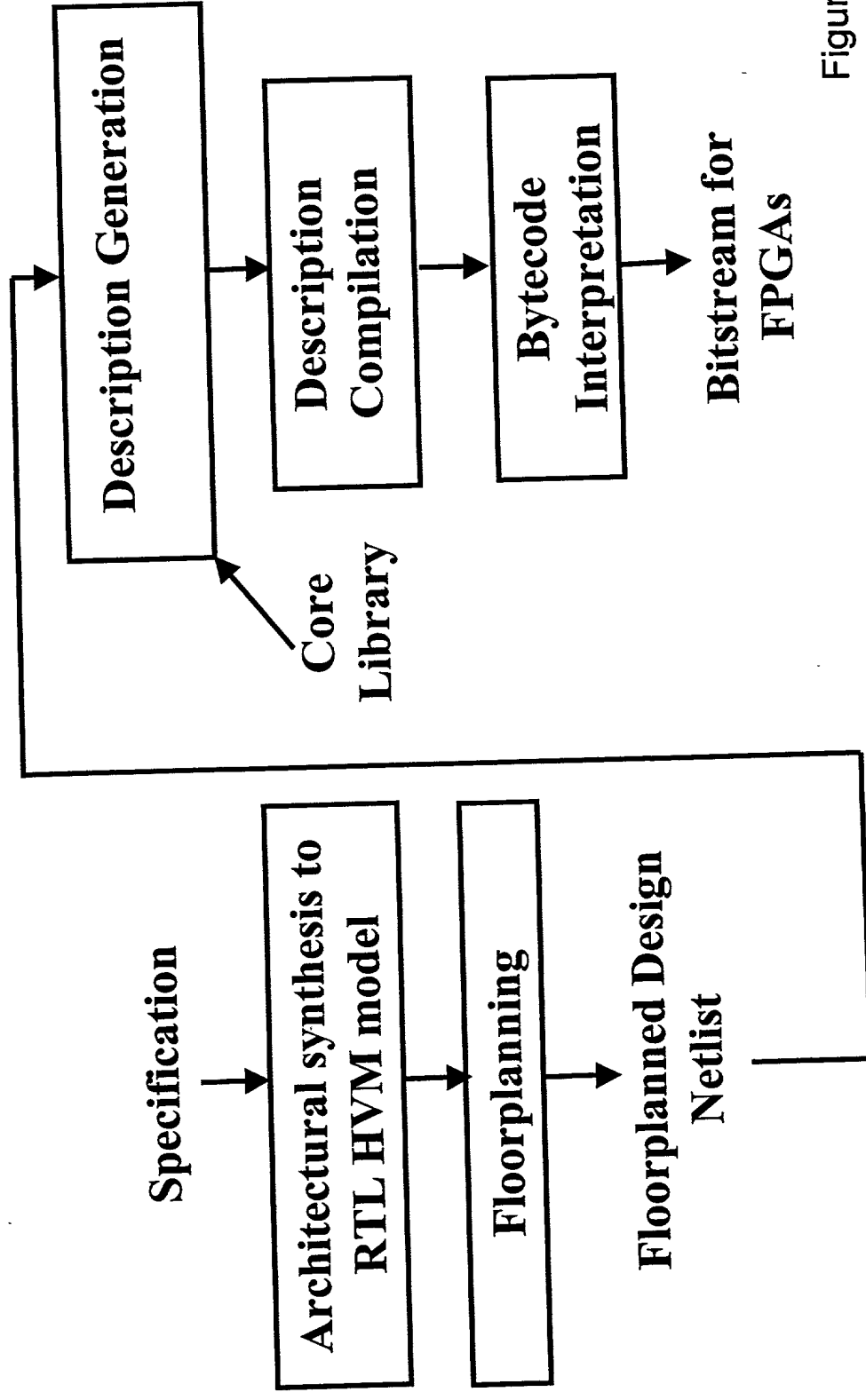


Figure 10

*Service Provider's Side*                      *Client's Side*

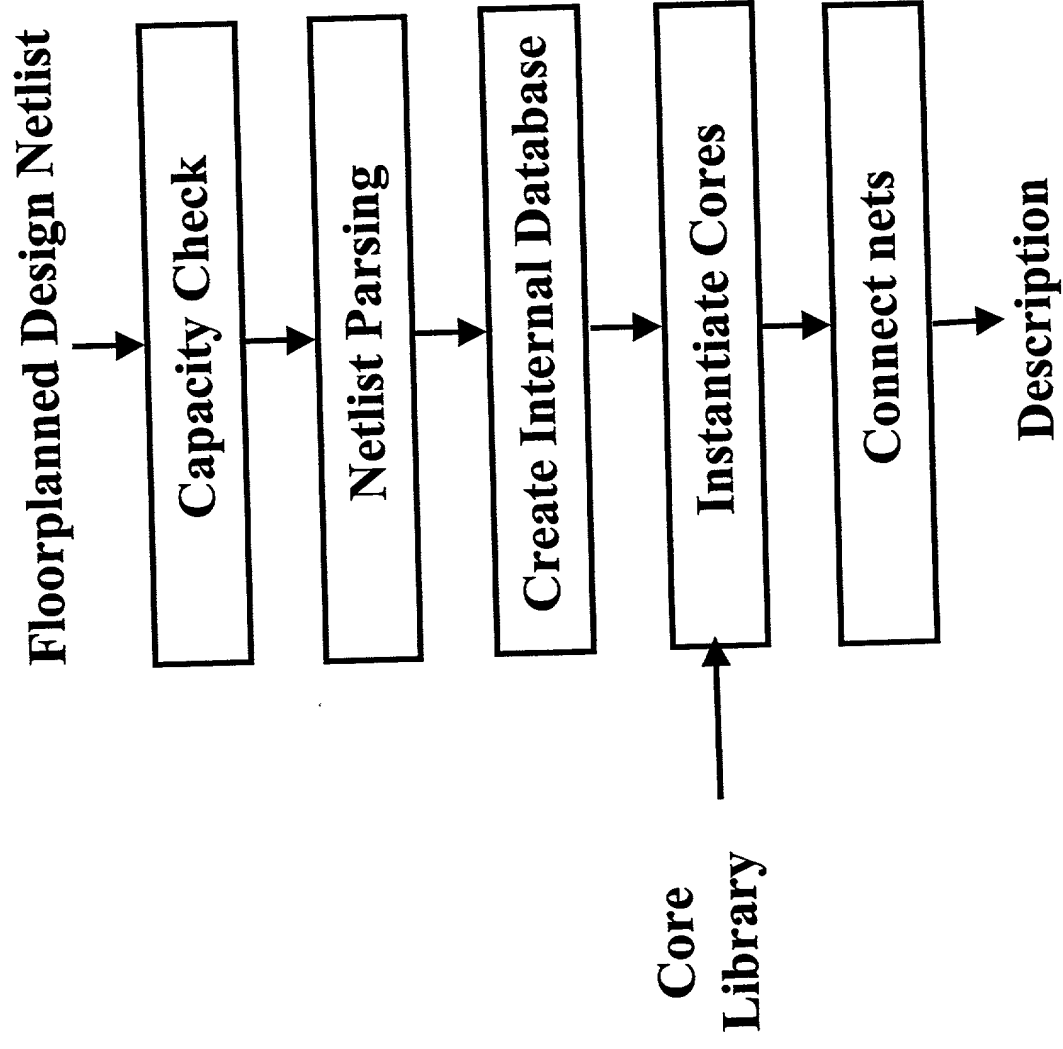


Figure 11

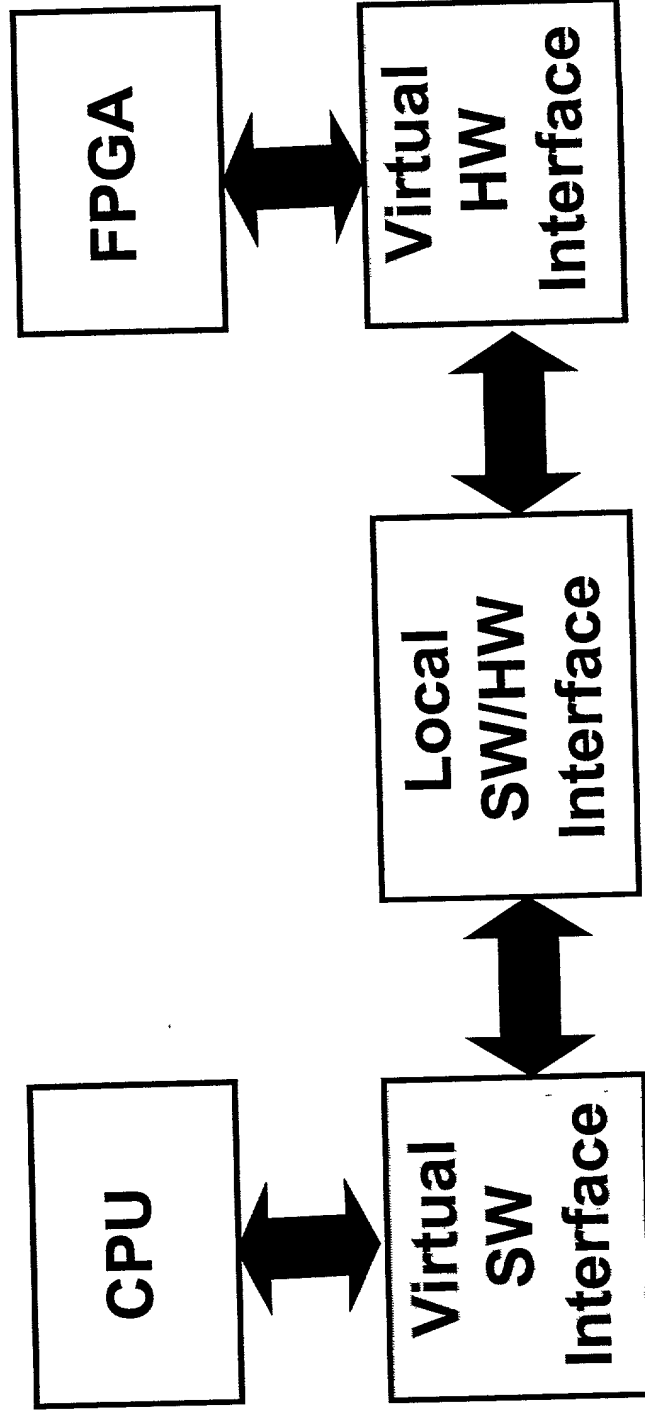


Figure 12

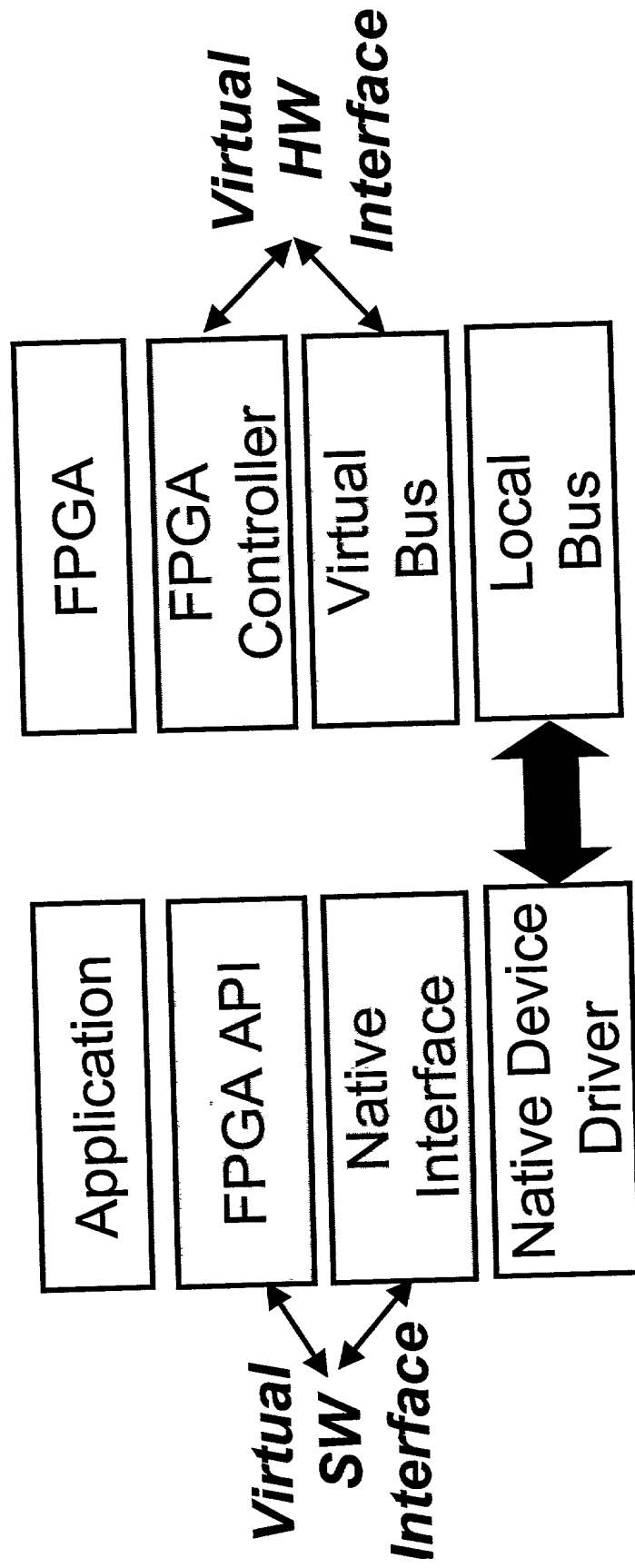


Figure 13

# An Abstract FPGA Model

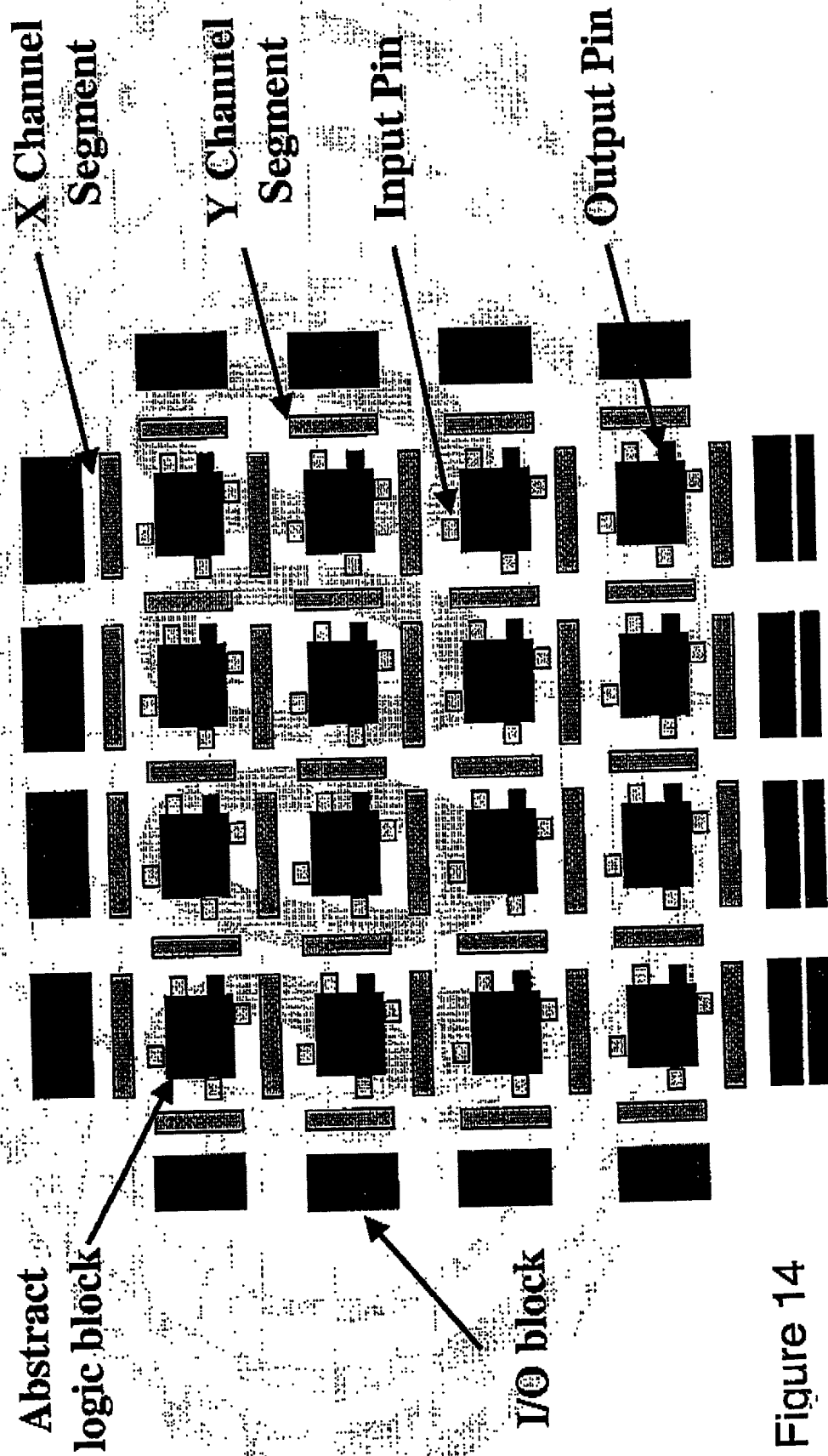


Figure 14